

New Generation Electronics Applied to Beam Position Monitors

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Abstract. Cellular telephones and global positioning system (GPS) satellite receivers are examples of modern rf engineering. Taking some inspiration from those designs, a precision signal-processor module for beam position monitors was developed. It features a heterodyne receiver (100 MHz to 1 GHz) with more than 90 dB dynamic range. Four multiplexed input channels are able to resolve signal differences lower than 0.0005 dB with good long-term stability. This corresponds to sub-micron resolution when used with a beam position pick-up with 40 mm free aperture. The paper concentrates on circuit design and modern dynamic testing methods, used first during development and later for production tests. The frequency synthesizer of the local oscillator, the phase-locked synchronous detector, and the low-noise preamplifier with automatic gain control are discussed. Other topics are design for immunity to electromagnetic interference to ensure reliable operation in an accelerator environment.

INTRODUCTION

Beam position monitors (BPMs) are essential diagnostic instruments in a particle accelerator and every accelerator project usually includes the development of a specific beam position monitoring system. Conventional beam position pick-ups use two or four electrodes (directional couplers or buttons) as position sensors. Beam position is a function of the amplitude difference of these electrodes' signals. The fundamental frequencies are specific to each particular accelerator and the power spectrum may extend to many GHz. Many methods for processing the beam position pick-up signals have been used or proposed in the past (1). Modern circular machines and storage rings, for example synchrotron light sources, have very high demands on the precision of these measurements. The objective is now to measure beam position with a resolution better than 1 μm . This requires measurement of the ratio of four electrical signals with a precision better than 0.0005 dB. The amplitude of the signals themselves could change over a range of more than three decades (> 60 dB) for different operating modes.

A UNIVERSAL BPM SIGNALPROCESSOR

We have taken the initiative to develop a universal BPM signal processor that would adapt easily to the frequency patterns of different accelerators. The starting point was a new BPM system designed by J. Hinkson (2) that is

optimized to measure the average closed-orbit position with high resolution. His primary application was transverse feedback and beam interlock systems near insertion devices in the Advanced Light Source (ALS) at Lawrence Berkeley National Laboratory.

Our BPM signal processor uses the same basic concept and architecture, but its center frequency is programmable anywhere between 100 MHz and 1 GHz. It tracks input signals over a limited frequency range (± 200 kHz, extension possible up to ± 1 MHz). Optional features are fast signal gating and a limited capability for single-turn measurements. Low cost, reliability, and simplicity of production were the other key requirements.

The central function of the signal processor is a receiver in the VHF/UHF frequency range. It was therefore a good idea to have a closer look at modern telecommunication equipment before starting our project. High-technology consumer products like cellular telephones and global positioning system (GPS) satellite receivers have started a revolution in modern rf technology. Complex systems are now being built on very small circuit boards, using novel integrated circuits functions and miniature passive components. They do not need heavy shielding enclosures.

Taking inspiration and components from those designs allowed us to shrink the processor module to a single-height Eurocard (100×160 mm). A built-in, pre-programmed frequency synthesizer for the down-converter makes the unit completely self-contained and independent of any external control or timing system. In its default operating mode, the user has only to connect the pick-up signals and the power supplies to obtain the normalized X and Y outputs. All intermediate coaxial connectors were eliminated by using on-board miniaturized bandpass filters, micro-strip low-pass filters, and adjustable attenuators. This improves the reliability of critical interconnections and lowers the component cost significantly.

Operating Principle

The BPM signal processor has four parallel input channels for the four input signals A to D. The input multiplexer switches sequentially from one input channel to the next. A single receiver measures the signal for each input channel in turn and stores its value in four corresponding analog memories. The voltages (V_A to V_D) in each of these memories are therefore proportional to the power levels of the original input signals. To normalize the readings (to make them independent of changing beam current), automatic gain control (AGC) is used to keep the sum $V_A + V_B + V_C + V_D$ constant.

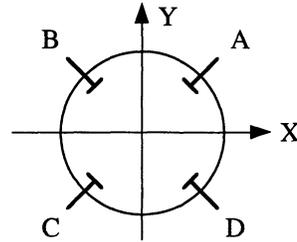
Sequential scanning and the use of a single receiver simplifies the circuits and has as major advantage, i.e., the gain for all channels is always identical. Gain changes due to temperature effects or component aging are eliminated by the

automatic gain control. The measurements are only valid if input conditions do not change during the scan. In practice, this is a very good method for beam position measurements of the average closed orbit.

The X and Y coordinates are calculated with a matrix of sum and difference analog circuits. They use the following algorithms for a typical position pick-up (with the four electrodes rotated at 45° with respect to the vertical axis).

$$X = K_x \frac{V_A + V_B - V_C - V_D}{V_A + V_B + V_C + V_D} \quad (\text{V/mm})$$

$$Y = K_y \frac{V_A - V_B - V_C + V_D}{V_A + V_B + V_C + V_D} \quad (\text{V/mm})$$



The calibration constants K_x and K_y of the beam position pick-up are an approximation and apply only to the center of the vacuum chamber.

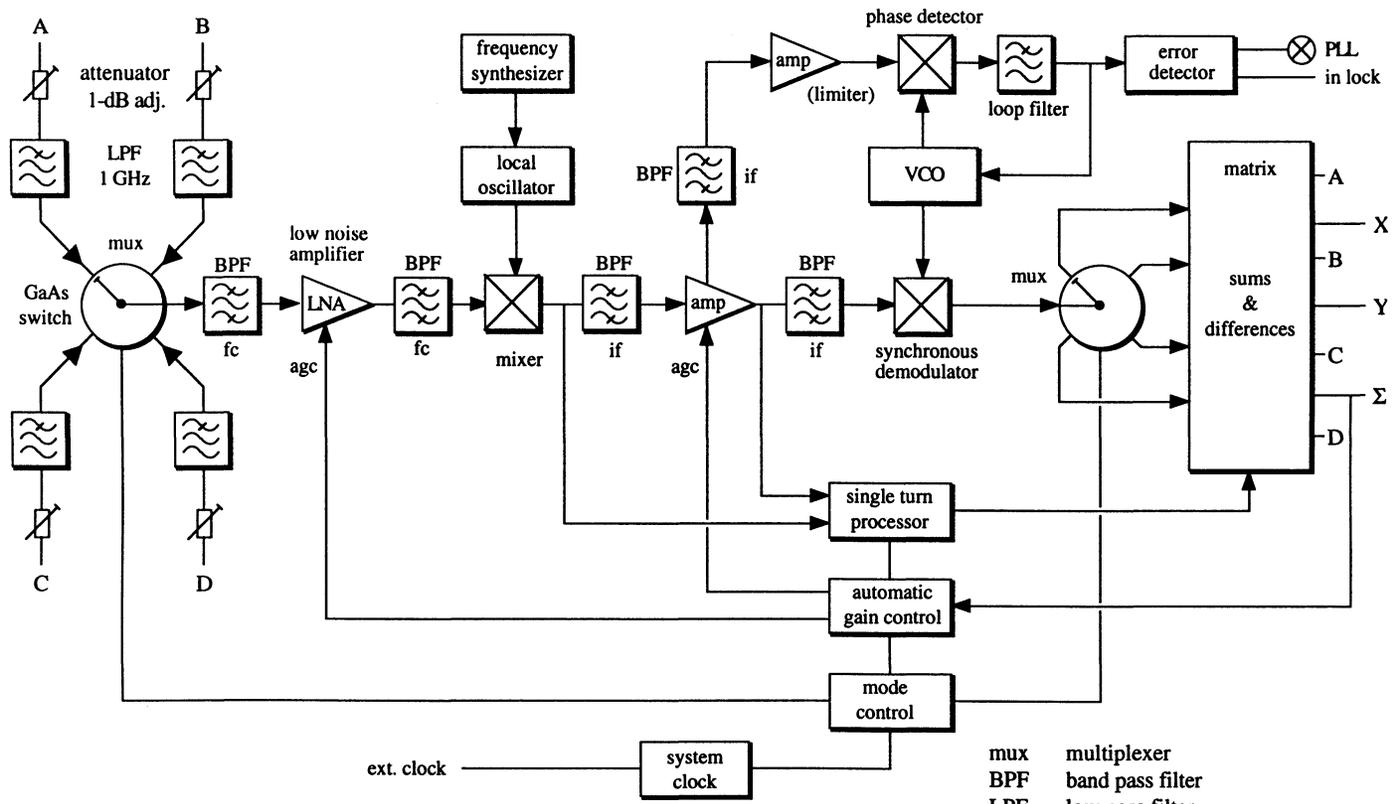
The basic operating principle, as described above, has been used for the first time at the NSLS storage ring (3). In the following chapters, design criteria for certain elements of the system will be discussed. A more complete description of the prototype for the ALS can be found in an earlier report (2).

Input Multiplexer

The block diagram (Fig. 1) shows 1-GHz low-pass filters in each of the four input channels. They are necessary to protect the GaAs switches from the very short, high-voltage pulses which are typical of wide-band pick-up signals. Stripline filters have been used before (4) for this function, but in our design they are folded up to occupy a very small area on the circuit board. Not shown on the diagram are the high-pass filters (7 MHz) which protect the switches from an accidental DC or low-frequency AC input. The attenuators (if required) reduce the signal power to the maximum level which the amplifier can accept. A 1-dB variable adjustment is used to equalize insertion loss in all four channels. The output impedance of the four channels, as seen by the switch, have to be matched to very tight tolerances.

Low-Noise Amplifier

This is a key element for the performance of the BPM signal processor. It has the dual function of low-noise amplifier and attenuator with a 50-dB gain



mux multiplexer
 BPF band pass filter
 LPF low pass filter
 VCO voltage controlled oscillator
 fc receiver centre frequency
 if intermediate frequency (21.4 MHz)

FIGURE 1. BPM signal processor simplified block diagram.

control range. More than 100-dB dynamic range is required, without gain compression, because gain compression anywhere in the signal path would change the calibration of the BPM signal processor as a function of input signal power.

Amplifiers with gain control have a tendency to change input admittance when changing gain. Considering the unavoidable matching errors of the input channels, this could be the cause of an unbalance in channel gain. This has to be avoided, because the resulting effect for the BPM signal processor is a zero offset which changes as a function of input signal power.

The requirements above are very different from the usual specifications of telecommunication equipment. It was therefore necessary to build a special amplifier with discrete transistors to cover the 100-MHz to 1-GHz frequency range and reach an acceptable compromise between conflicting demands.

Local Oscillator and Frequency Converter

An active mixer is used as down-converter to the 21.4-MHz intermediate frequency (IF). This is another critical element in the signal chain, where gain compression is likely to limit the available dynamic range. Thanks to the AGC in the preamplifier, the signal amplitude changes are already reduced at this point.

The local oscillator should not contribute any significant amplitude or phase noise to the processed signals. A frequency synthesizer (Fig. 2) is used as a source. It consists of a voltage-controlled oscillator (VCO) with programmable divider (5) phase locked to a reference frequency (f_{ref}). A 17-bit serial word from a plug-in F-key module selects the divider ratio for a specific receiver center frequency. Spectral purity of the local oscillator depends on the choice of the reference frequency and the dynamic response of the phase-locked loop (PLL).

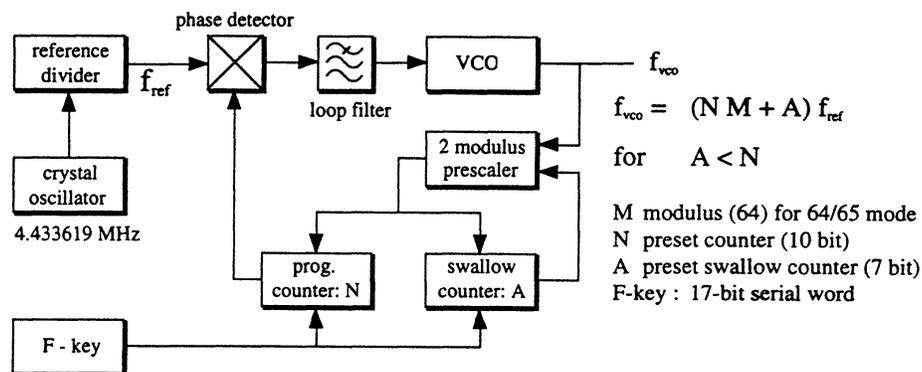


FIGURE 2. Frequency synthesizer.

IF Amplifier and Demodulator

The integrated circuit* used as an IF amplifier and demodulator is designed for television applications. We had to add discrete transistor stages at input and output of the IF amplifier to match the IF filters and improve the gain compression limits. The IF bandwidth (Fig. 3) can be tuned from 200 kHz to 2MHz to suit any particular application. The bandwidth is large enough to allow a fast step response when switching from one input channel to the next. Sidebands at the revolution frequency are rejected in order to make the detector see the same kind of signal independently of the accelerator operating mode: multibunch or single bunch.

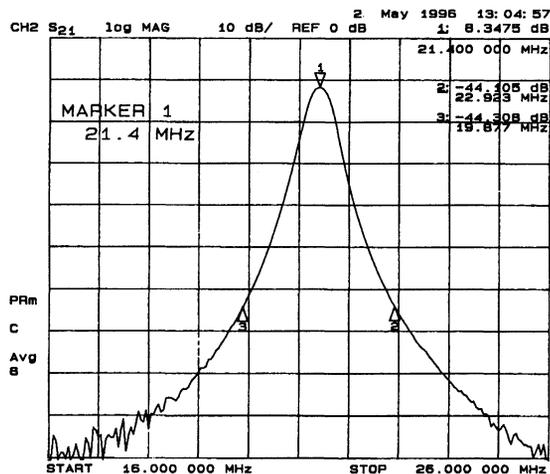


FIGURE 3. Frequency response of IF amplifier (BPM processor for ALS). Bandwidth (-3 dB) = 434 kHz. Markers indicate the sidebands for a revolution frequency of 1523.4 kHz.

Synchronous detection of the IF signal requires a reference frequency. This reference is generated by a VCO. A phase detector compares the reference with a filtered sample of the carrier frequency and controls the VCO in a PLL. The dynamic response of the PLL is controlled by the loop filter.

If the pick-up signals applied to the BPM signal processor inputs are not in phase, switching from one input channel to the next would produce sudden phase jumps of up to 180° . Even a fast PLL would encounter difficulties, and this would seriously limit the maximum scanning frequency.

Many of the BPM systems presently in use require precise phase matching on all signal cables coming from the pick-ups. We preferred to solve this problem

*LM1823, National Semiconductor Corporation

in a different way. Our loop filter has an electronic switch (not shown in Fig. 1) which reduces the time constants during the 10 μ s after channel switching. This allows the receiver to settle on a new signal level; as a result, phase errors up to 180° are tolerated.

ELECTROMAGNETIC INTERFERENCE

The BPM signal processor will be used in machine protection interlocks, where reliable operation is extremely important. In addition to shielding the sensitive parts of the board, a number of special precautions have been incorporated in the design to improve immunity to electromagnetic interference.

- The coaxial inputs pass via an uninterrupted ground plane before connecting to the circuit board.
- All other input and output connections have low-pass filters to keep the interference outside and limit the frequency response to what is absolutely necessary.
- All control inputs have 10-ms low-pass-filter time constants.
- Each circuit function on the board is specifically designed to be insensitive to frequencies outside its normal operating range. This is particularly important for operational amplifiers which have a tendency to demodulate rf signals and, as a result, produce erroneous DC output.

DYNAMIC TESTING

The different rf circuit and filter functions of the BPM signal processor require alignment and dynamic testing during development and in the final production phase. Conventional rf circuits have special coaxial test connectors. Considering the high packing density on our printed circuit, this was not a desirable solution. Instead, after some initial experimenting, we developed a special miniature rf test set. On the board, this required simply two plated-through holes at a distance of 0.1 inch, with one of them connected to the ground plane. The coaxial test probes have two corresponding test pins, consisting of gold-plated, spring-loaded contacts. For use with a network analyzer (Hewlett Packard HP8753D), a matching calibration set (open, short, and 50- Ω load) permits us to establish the correction constants, which take care of the small residual discontinuity of these connections. The test set is used for measuring impedance and transfer functions (Fig. 3) for frequencies up to 3 GHz.

Testing the transient response of feedback (AGC) and phase-locked loops uses the same type of test connections, but requires a different instrument set-up. Generally speaking, the method consists of injecting a square wave modulated stimulus, most often a DC current, in a suitable summing junction of the loop under test. The transient response is observed with an oscilloscope at another test

point and can be optimized by tuning the different elements of the loop filters or phase correction networks.

A spectrum analyzer (Anritsu MS2601B) is used to measure the signal at different points of the signal path. It can determine the 1-dB gain compression point and the saturation limit for every location along the signal processing chain. Spectral purity and stability of the local oscillator is verified with the spectrum analyzer.

A special test generator has been built to simulate fast pick-up signal pulses with repetition rates up to 15 MHz. This allows testing of the BPM signal processor by simulating different filling patterns and single-bunch mode. The peak amplitude of the generator is at present limited to 22 V and is therefore insufficient to test the upper limit of the dynamic range in these modes.

An automated test bench for final testing and certification of the BPM signal processor is presently under development. It uses a programmable continuous wave (CW) signal generator (Marconi Instruments 2022D) as a signal source. A precision 4-way power splitter and four specially designed precision attenuators with remote switching control prepare the four input signals. A Macintosh computer with a 16-bit ADC, multiplexer, and control interface (National instruments NB-MIO-16X) runs a specially developed LabVIEW application program (6). The test bench establishes a test report, recording noise and offset errors in all quadrants over the entire dynamic range ($> 80\text{dB}$)

The noise spectrum of X and Y outputs, as a function of input signal power, is recorded with an FFT spectrum analyzer (Stanford Research Systems SR760).

Performance Figures

The following dimensional data refer to calibration with a “reference” pick-up: Sensitivity in X and Y plane = 5%/mm (40-mm aperture).

- Noise → X and Y signal (for the first 40 dB of the dynamic range):
 less than $1.5\ \mu\text{m}$ (rms) for a bandwidth of 0 to 1 kHz
 less than $0.5\ \mu\text{m}$ (rms) for a bandwidth of 0 to 100 Hz
- Zero stability → X and Y zero drift less than $0.5\ \mu\text{m}$ during 10 hours
- Linearity → Over 60 dB of input signal range:
 less than $\pm 5\ \mu\text{m}$ error within $\pm 0.5\text{mm}$ of center
 less than $\pm 10\ \mu\text{m}$ error within $\pm 3\text{mm}$ of center

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